DATA SHEET

SA56615-XX; SA56616-XX

CMOS system reset with adjustable delay time

Product data

2002 Mar 25

**Philips
Semiconductors**

PHILIPS

CMOS system reset with adjustable delay time

SA56615-XX;
SA56616-XX

GENERAL DESCRIPTION

The SA56616-XX and SA56615-XX CMOS system resets have low consumption current of typically 1.0 µA and high precision detection voltage within ±2%. The delay time is adjusted by an external capacitor working in conjunction with the on-chip delay network. The SA56615-XX and SA56616-XX have different output configurations to accommodate a wide variety of microprocessors and logic devices. The SA56615-XX incorporates a low side open-drain output topology which requires a pull-up resistor to V_{DD}, while the SA56616-XX incorporates an active push-pull totem pole output topology comprised of complimentary P-channel and N-channel FETs.

The resets operate over a wide operating supply voltage range from 0.7 V to 10 V. Reset detection voltages are available at 0.9 V, 1.8 V, 1.9 V, 2.0 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.2 V, 4.3 V, 4.4 V, 4.5 V, 4.6 V and 4.7 V. Other thresholds are offered upon request at 100 mV increments from 0.9 V to 6.0 V. The device comes in the small SOT23-5 package.
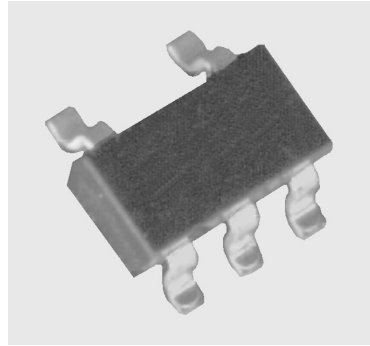
FEATURES

- Super low supply current: typically 1.0 µA ($V_{DD} = V_S + 1$ V)

- Operating supply voltage range: 0.7 V to 10 V

- High precision detection voltage: ±2%

- Detection voltage: 0.9 V, 1.8 V, 1.9 V, 2.0 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.2 V, 4.3 V, 4.4 V, 4.5 V, 4.6 V, and 4.7 V

- Other detection threshold voltages available at 100 mV steps from 0.9 V to 6.0 V

- User adjustable reset delay time

- Versatile output configurations:
  - SA56615-XX: open-drain
  - SA56616-XX: N-channel/P-channel push-pull

APPLICATIONS

- Microprocessor and logic circuit reset

- Battery voltage level detection

- Battery backup and switching circuits

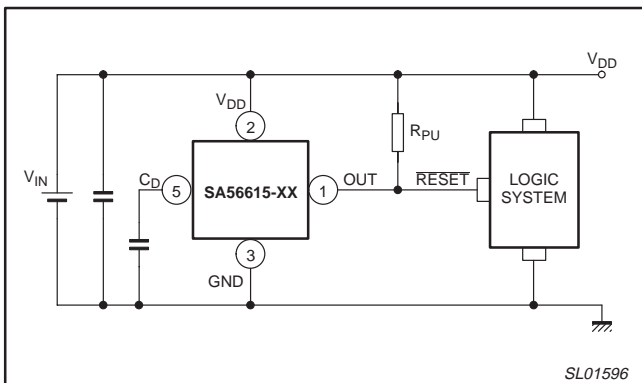- Adjustable time delay circuits

SIMPLIFIED SYSTEM DIAGRAMS

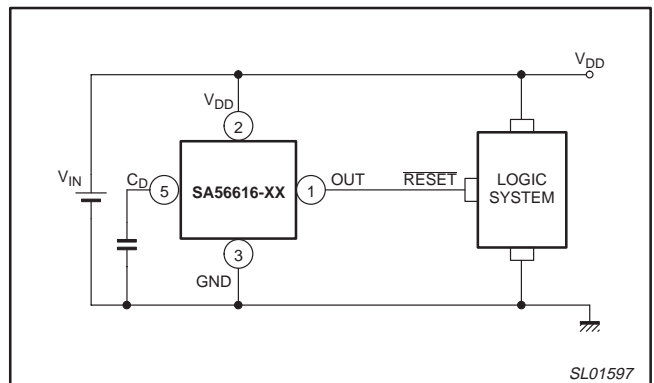**Figure 1. SA56615-XX simplified system diagram.**

Figure 2. SA56616-XX simplified system diagram.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | TEMPERATURE RANGE |
	NAME	DESCRIPTION	
SA56615-**XX**D	SOT23-5, SOT25, SO5	plastic small outline package; 5 leads (see dimensional drawing)	−40 to +85 °C
SA56616-**XX**D	SOT23-5, SOT25, SO5	plastic small outline package; 5 leads (see dimensional drawing)	−40 to +85 °C

NOTE:
The device has 15 voltage output options, indicated by the XX on
the 'Type number'.

XX	VOLTAGE (Typical)
09	0.9 V
18	1.8 V
19	1.9 V
20	2.0 V
27	2.7 V
28	2.8 V
29	2.9 V
30	3.0 V
31	3.1 V
42	4.2 V
43	4.3 V
44	4.4 V
45	4.5 V
46	4.6 V
47	4.7 V

PIN CONFIGURATION
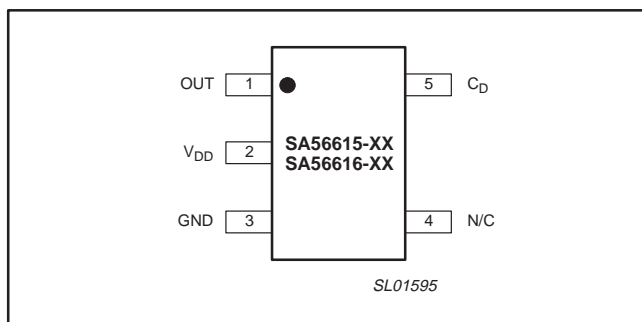
Figure 3. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	OUT	Output. $\overline{\text{RESET}}$ Active-LOW.
2	V_{DD}	Power supply voltage.
3	GND	Ground. Negative supply.
4	N/C	No connection.
5	C_D	Time delay pin. Delay adjusted by capacitor to ground.

MAXIMUM RATINGS

SYMBOL	PARAMETER		MIN.	MAX.	UNIT
$V_{DD(max)}$	Power supply voltage		–	+12	V
V_{OUT}	Output voltage	SA56615-XX	$V_{SS} + 0.3$	12	V
		SA56616-XX	$V_{SS} - 0.3$	12	V
I_{OUT}	Output current		–	70	mA
$V_{i(CD)}$	C_D pin input voltage		$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
T_{amb}	Ambient operating temperature		–40	85	°C
T_{stg}	Storage temperature		–40	125	°C
P	Power dissipation		–	150	mW

ELECTRICAL CHARACTERISTICS

$T_{amb} = 25$ °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{hys}	Hysteresis voltage		$V_S \times 0.03$	$V_S \times 0.05$	$V_S \times 0.07$	V
$V_S/\Delta T$	Detection voltage temperature coefficient	-40 °C $\leq T_{amb} \leq 85$ °C	–	±0.01	–	%/°C
I_{SS1}	Supply current 1	$V_{DD} = (V_{SL}) - 0.13$ V	–	4	8	µA
I_{SS2}	Supply current 2	$V_{DD} = (V_{SL}) + 2.0$ V	–	1.2	3.6	µA
I_{OUT1}	Output current 1	Nch: $V_{DS} = 0.05$ V; $V_{DD} = 0.7$ V	0.01	0.05	–	mA
I_{OUT2}	Output current 2	$V_{DD} = 1.5$ V; Nch: $V_{DS} = 0.05$ V; $V_{DD} = 1.5$ V	1.0	2.0	–	mA
I_{OUT3}	Output current 3	$V_{DD} = 4.5$ V; Pch: $V_{DS} = -2.1$ V (Note 1)	1.0	2.0	–	mA
V_{TCD}	Delay threshold voltage	$V_{DD} = (V_{SL}) \times 1.1$ V	$V_{DD} \times 0.4$	$V_{DD} \times 0.5$	$V_{DD} \times 0.6$	V
I_{CD1}	Delay output current 1	$V_{DS} = 0.1$ V; $V_{DD} = 0.7$ V	2	30	–	µA
I_{CD2}	Delay output current 2	$V_{DS} = 0.5$ V; $V_{DD} = 0.7$ V	200	800	–	µA
V_{DDL1}	Minimum supply voltage 1	$V_{OUT} \leq 0.1$ V; $T_{amb} = 25$ °C	–	0.55	0.70	V
V_{DDL2}	Minimum supply voltage 2	$V_{OUT} \leq 0.1$ V; -40 °C $\leq T_{amb} \leq 85$ °C	–	0.65	0.80	V
R_D	Delay C_D Pin Resistance		0.5	1.0	2.0	MΩ
I_{LEAK}	Output leakage current	$V_{DD} = 10$ V; $V_{CD} = 10$ V; $V_{DS} = 10$ V	–	–	0.1	µA

NOTE:
1. Output current 3 is SA56616-XX CMOS push-pull configuration only.

TYPICAL PERFORMANCE CURVES

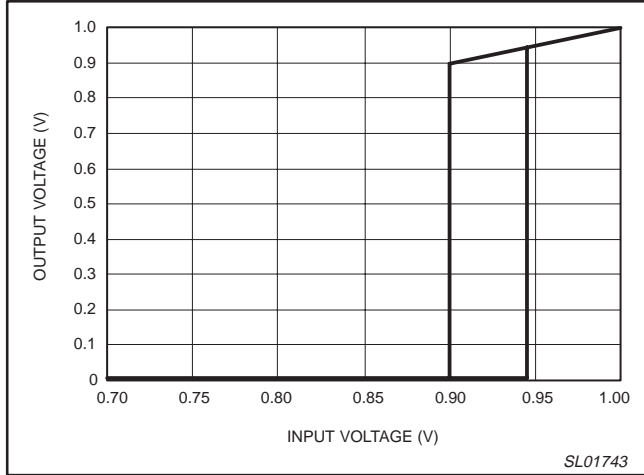**NOTE:** Typical characteristics for SA56616-09

Figure 4. Output voltage versus input voltage.

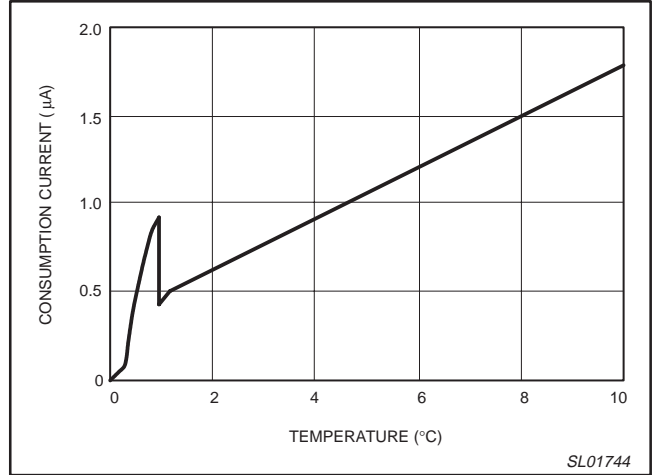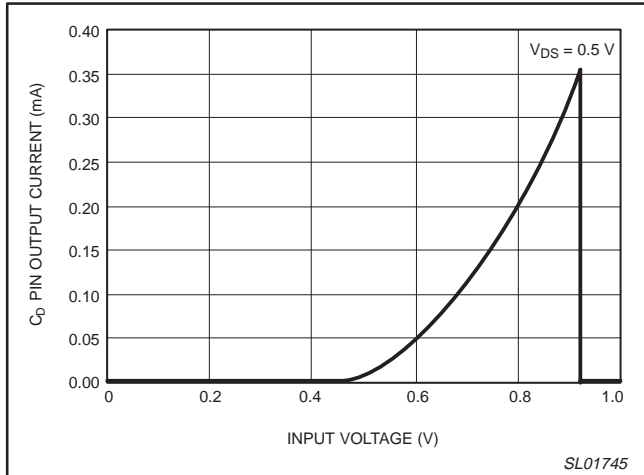Figure 5. Consumption current versus input voltage.

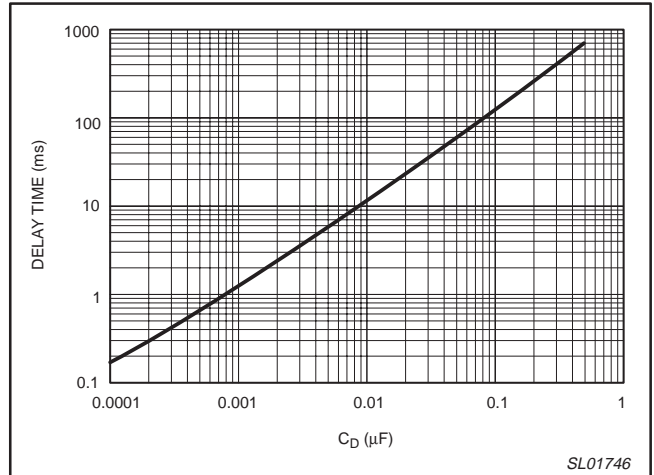Figure 6. C$_D$ pin output current versus input voltage.

Figure 7. Delay time versus C$_D$.

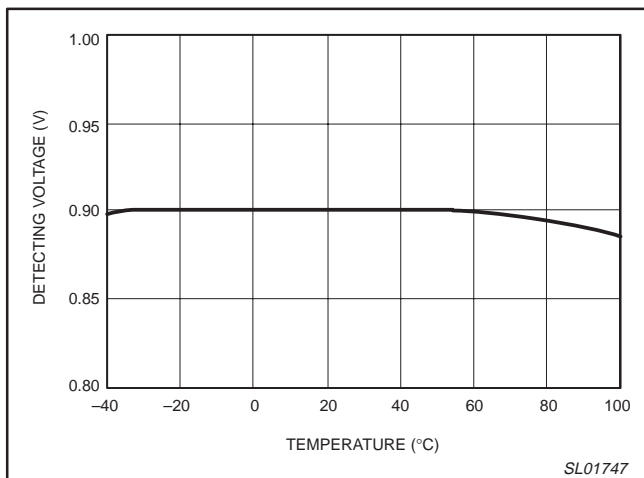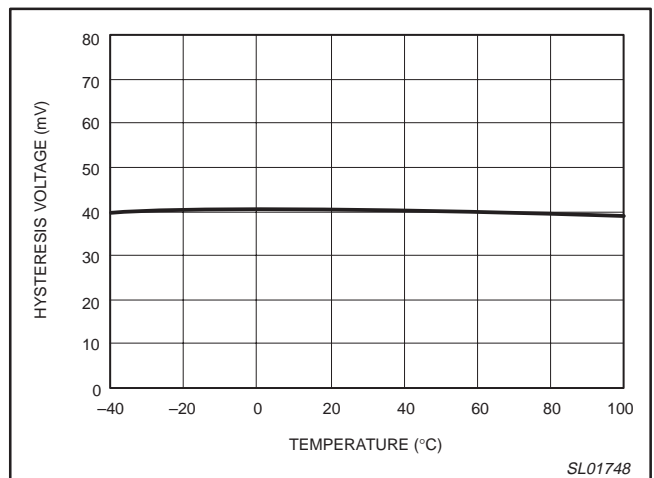Figure 8. Detection voltage versus temperature.

Figure 9. Hysteresis voltage versus temperature.

TYPICAL PERFORMANCE CURVES (continued)
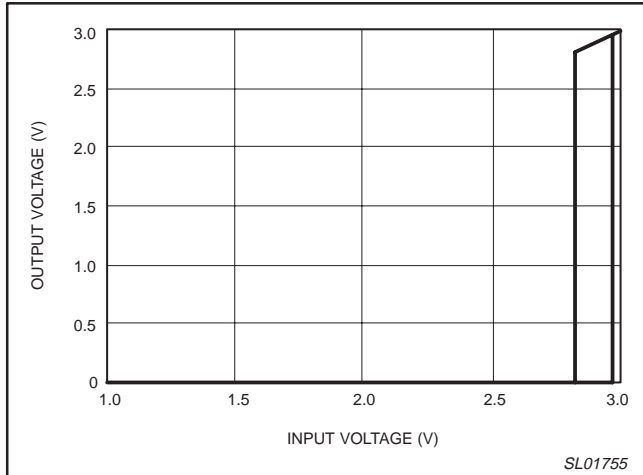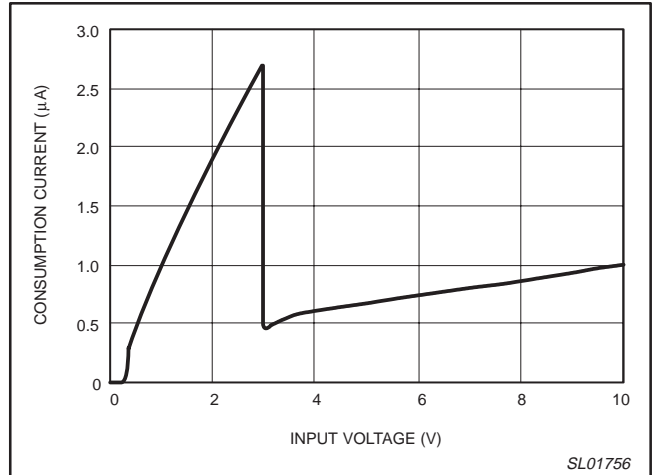**NOTE:** Typical characteristics for SA56616-09
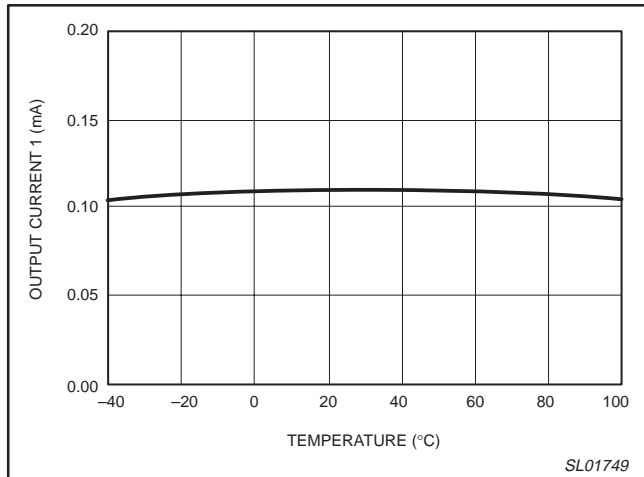
Figure 10. Output current 1 versus temperature.
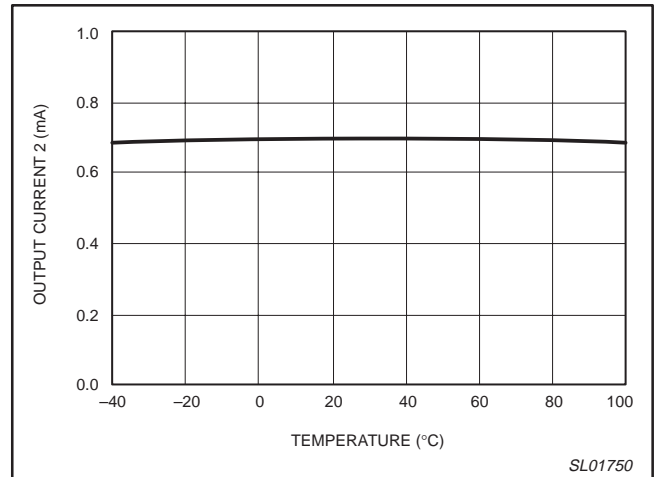
Figure 11. Output current 2 versus temperature.
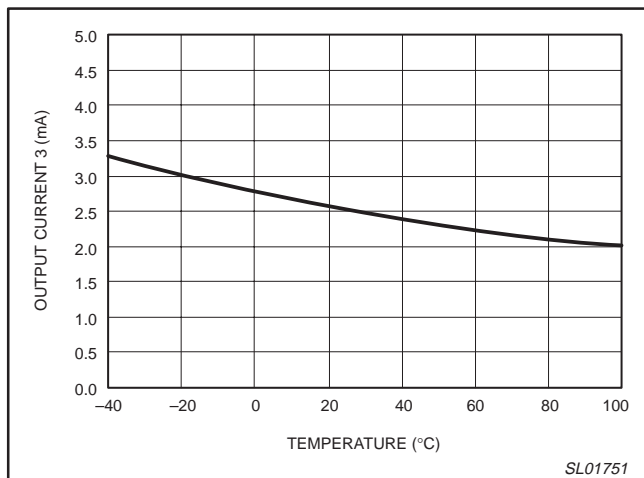
Figure 12. Output current 3 versus temperature.
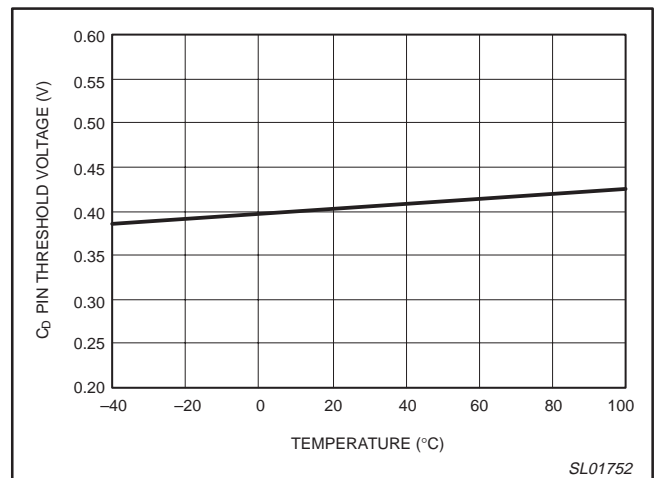
Figure 13. C$_D$ pin threshold voltage versus temperature.
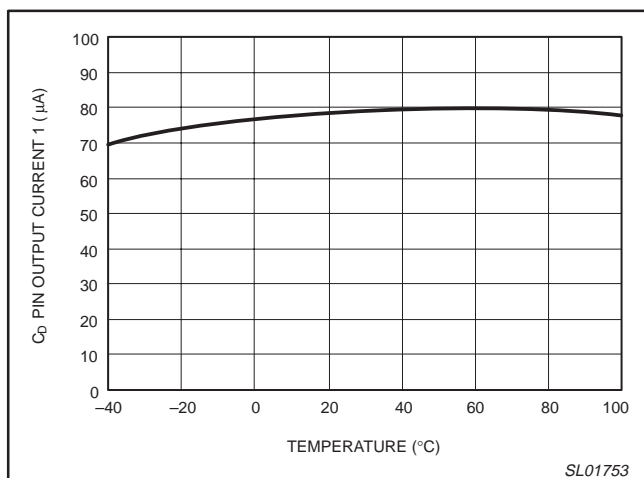
Figure 14. C$_D$ pin output current 1 versus temperature.
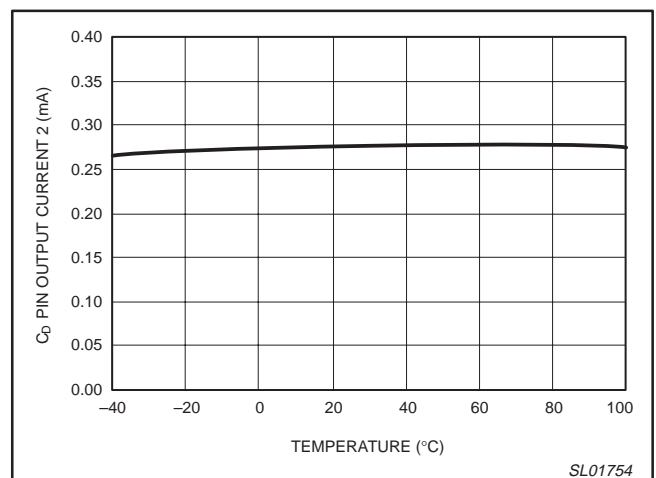
Figure 15. C$_D$ pin output current 2 versus temperature.

TYPICAL PERFORMANCE CURVES (continued)
NOTE: Typical characteristics for SA56616-28

Figure 16. Output voltage versus input voltage.

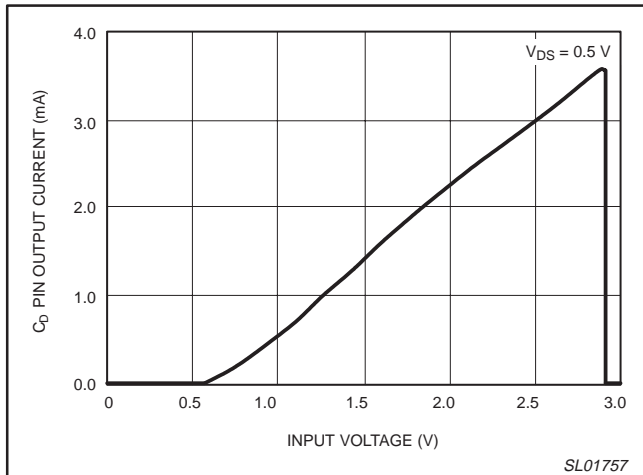**Figure 17. Consumption current versus input voltage.**

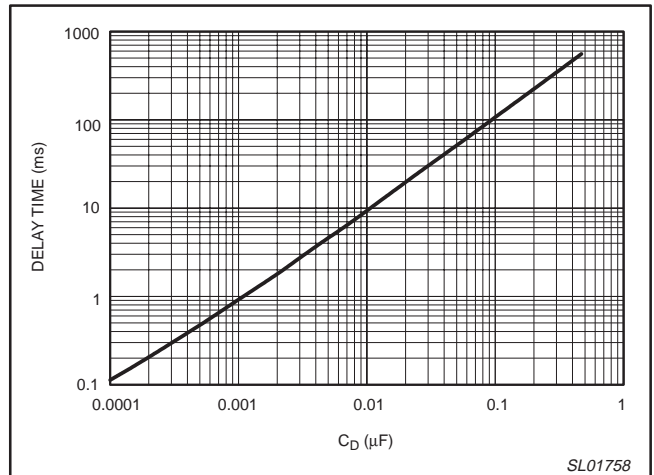**Figure 18. C$_D$ pin output current versus input voltage.**
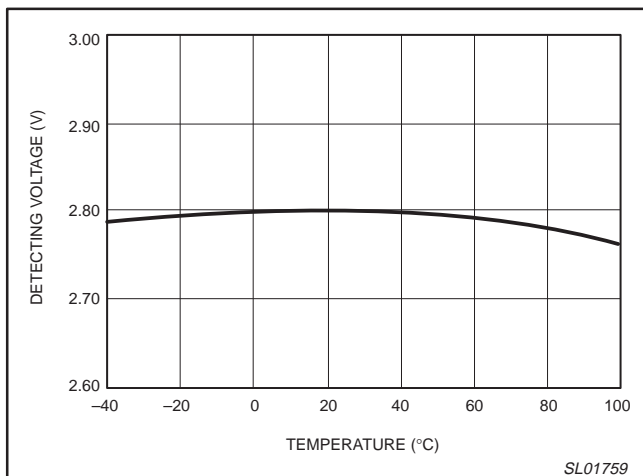

Figure 19. Delay time versus C$_D$.

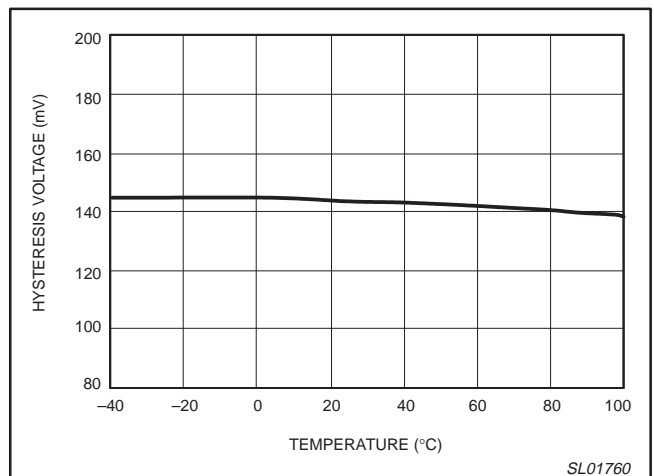**Figure 20. Detection voltage versus temperature.**

Figure 21. Hysteresis voltage versus temperature.

TYPICAL PERFORMANCE CURVES (continued)

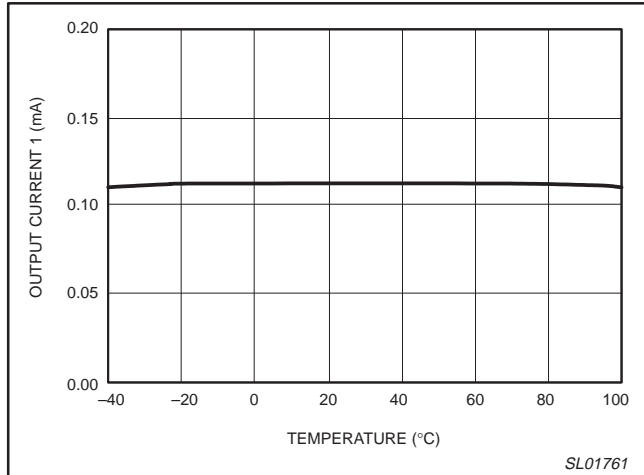**NOTE:** Typical characteristics for SA56616-28
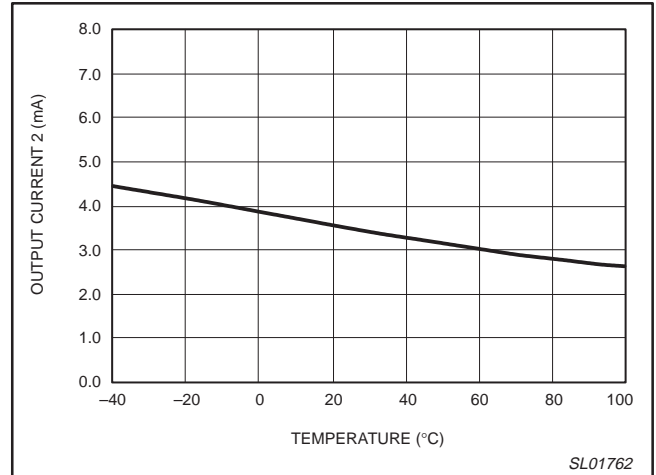
Figure 22. Output current 1 versus temperature.
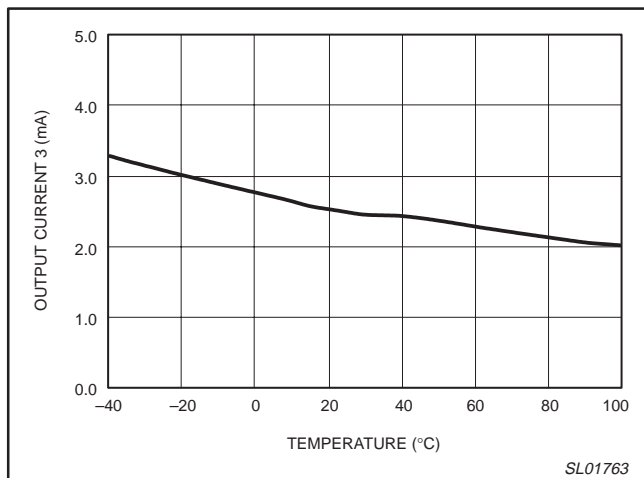
Figure 23. Output current 2 versus temperature.

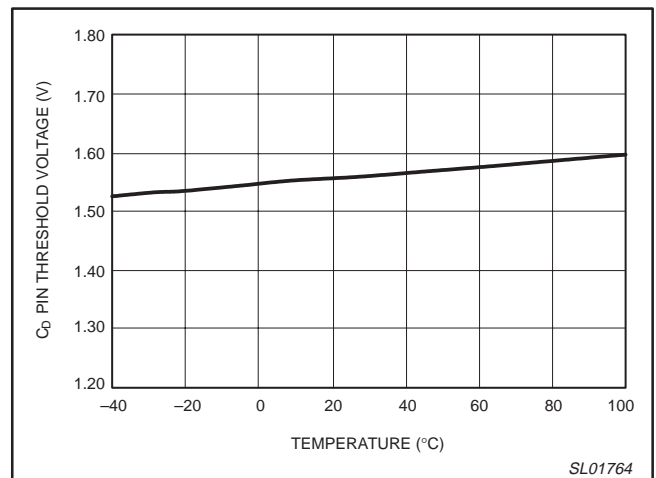**Figure 24. Output current 3 versus temperature.**

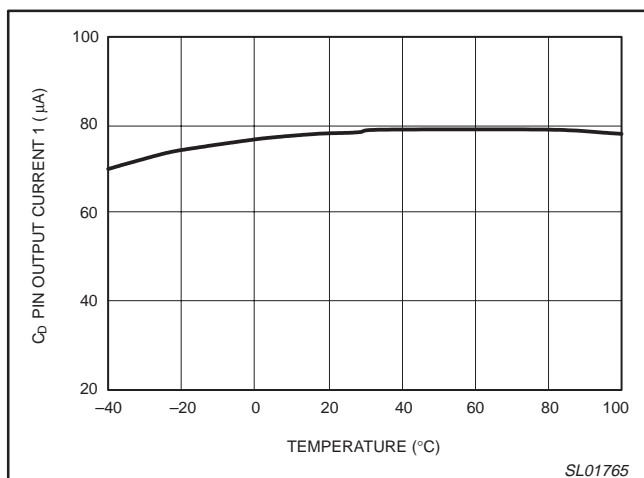**Figure 25. C$_D$ pin threshold voltage versus temperature.**

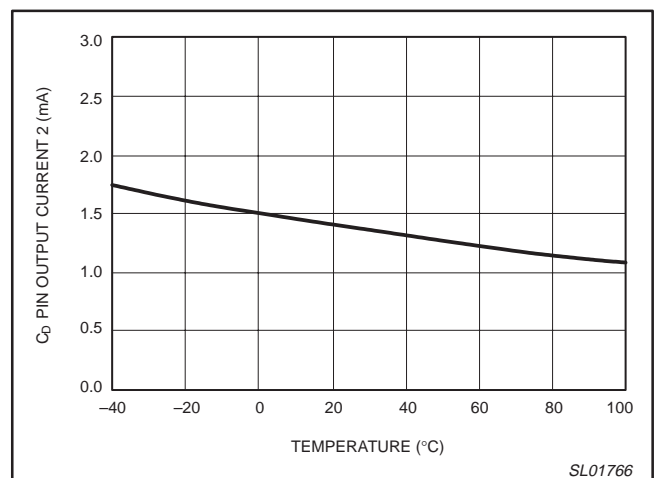**Figure 26. C$_D$ pin output current 1 versus temperature.**

Figure 27. C$_D$ pin output current 2 versus temperature.

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TYPICAL PERFORMANCE CURVES *(continued)*
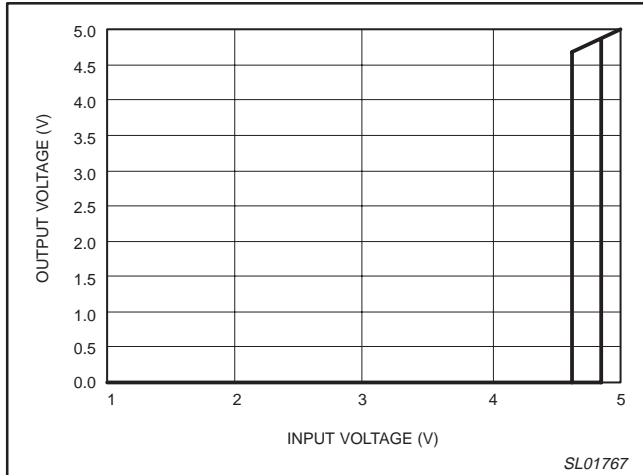**NOTE:** Typical characteristics for SA56616-46

Figure 28. Output voltage versus input voltage.
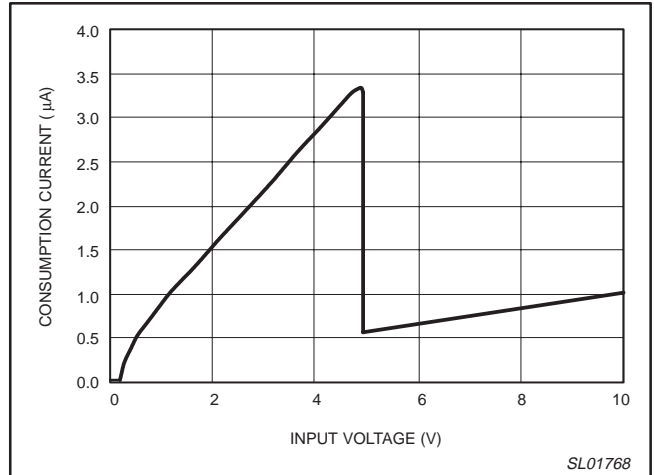

Figure 29. Consumption current versus input voltage.
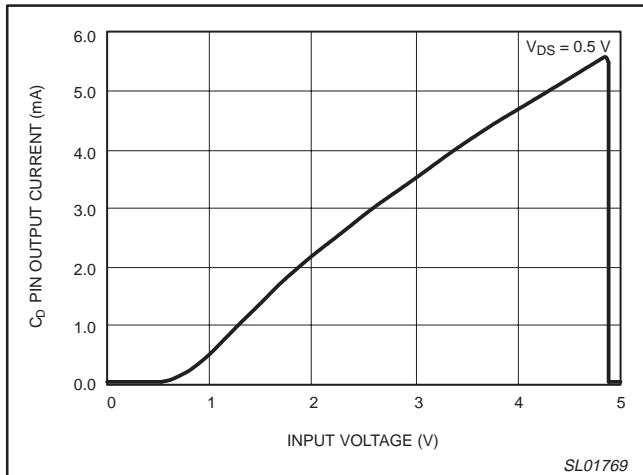

Figure 30. C_D pin output current versus input voltage.

Figure 31. Delay time versus C_D.

Figure 32. Detection voltage versus temperature.

Figure 33. Hysteresis voltage versus temperature.

TYPICAL PERFORMANCE CURVES *(continued)*
NOTE: Typical characteristics for SA56616-46

Figure 34. Output current 1 versus temperature.

Figure 35. Output current 2 versus temperature.

Figure 36. Output current 3 versus temperature.

Figure 37. C_D pin threshold voltage versus temperature.

Figure 38. C_D pin output current 1 versus temperature.

Figure 39. C_D pin output current 2 versus temperature.

TYPICAL PERFORMANCE CURVES (continued)

NOTE: Typical characteristics for SA56615-09

Figure 40. Output voltage versus input voltage.

Figure 41. Consumption current versus input voltage.

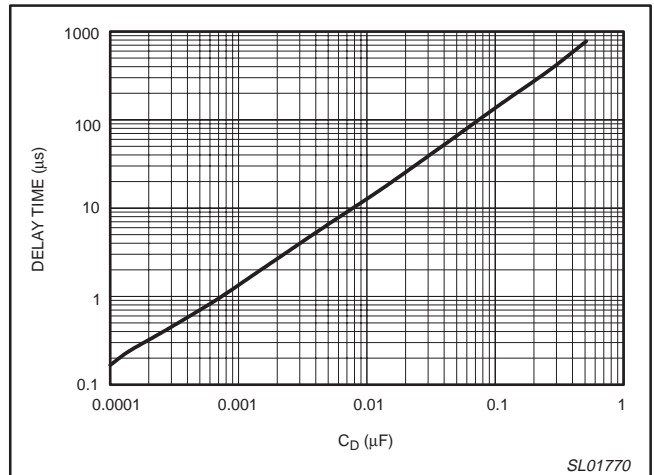**Figure 42. C$_D$ pin output current versus input voltage.**
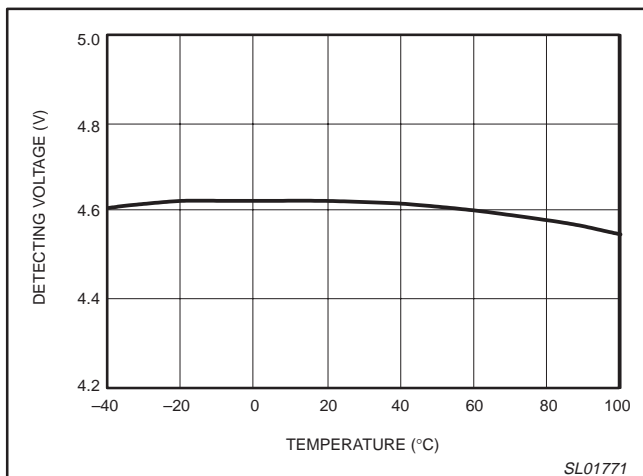

Figure 43. Delay time versus C$_D$.

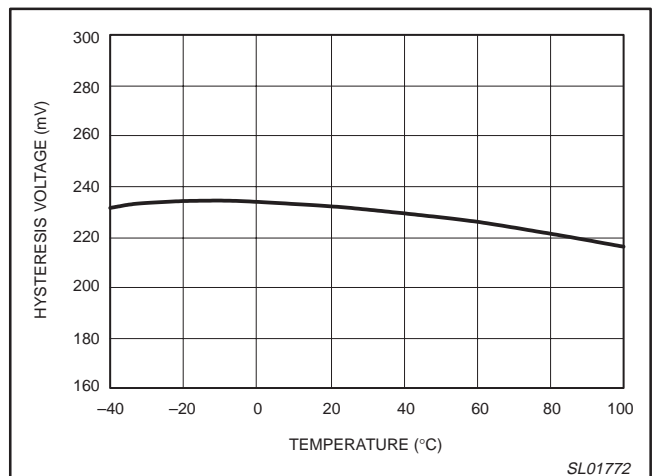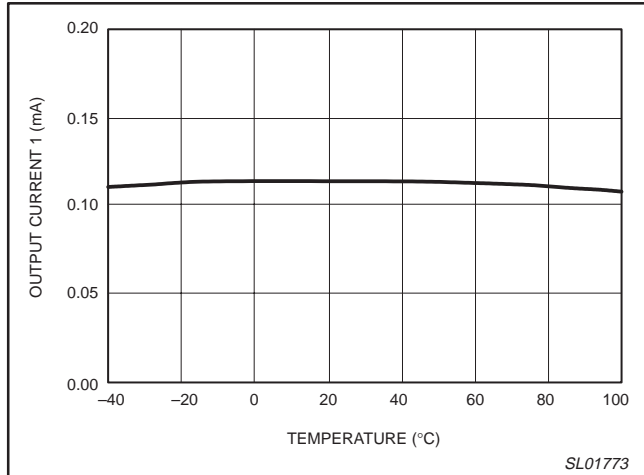**Figure 44. Detection voltage versus temperature.**

Figure 45. Hysteresis voltage versus temperature.

TYPICAL PERFORMANCE CURVES (continued)
NOTE: Typical characteristics for SA56615-09
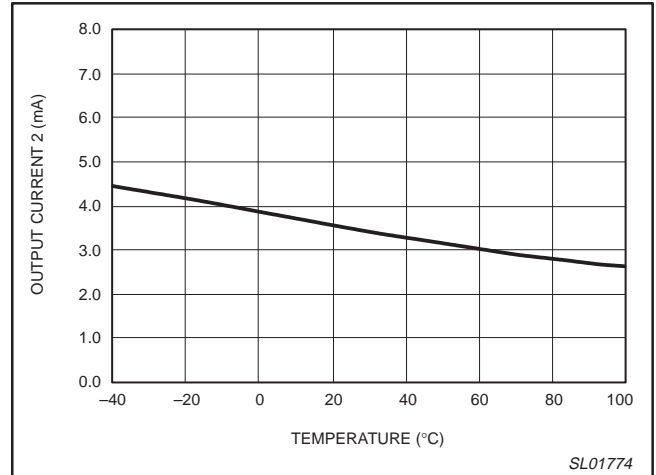

Figure 46. Output current 1 versus temperature.
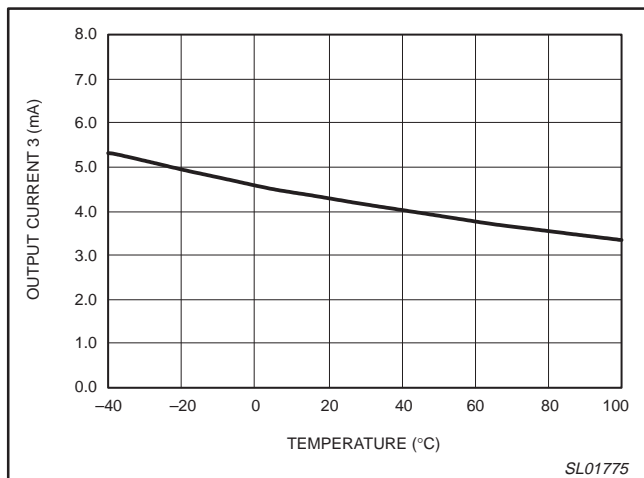

Figure 47. Output current 2 versus temperature.
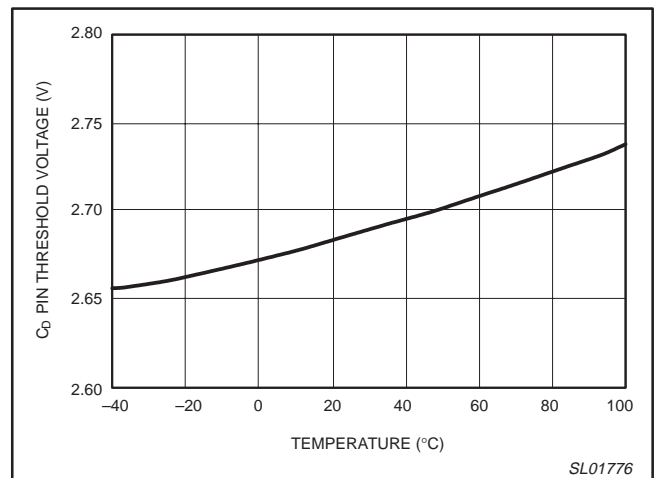

Figure 48. C$_D$ pin threshold voltage versus temperature.

Figure 49. C$_D$ pin output current 1 versus temperature.

Figure 50. C$_D$ pin output current 2 versus temperature.

TYPICAL PERFORMANCE CURVES *(continued)*
NOTE: Typical characteristics for SA56615-28
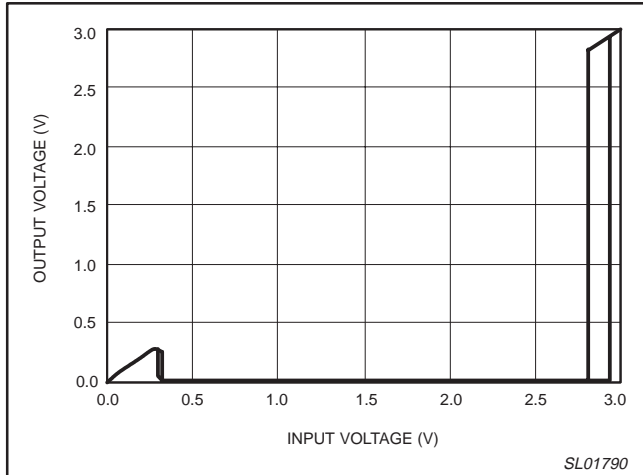
Figure 51. Output voltage versus input voltage.
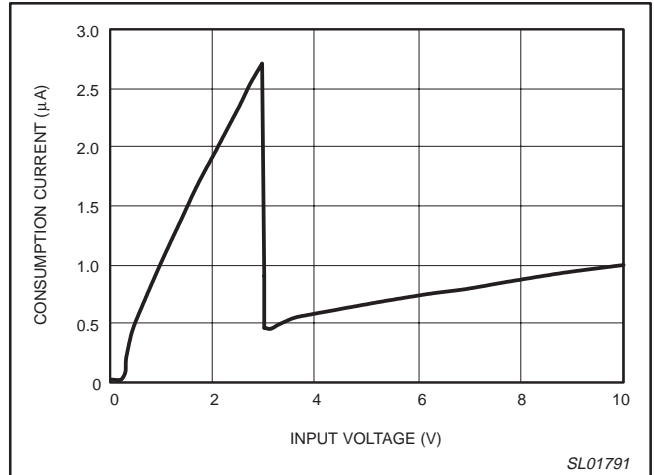
Figure 52. Consumption current versus input voltage.
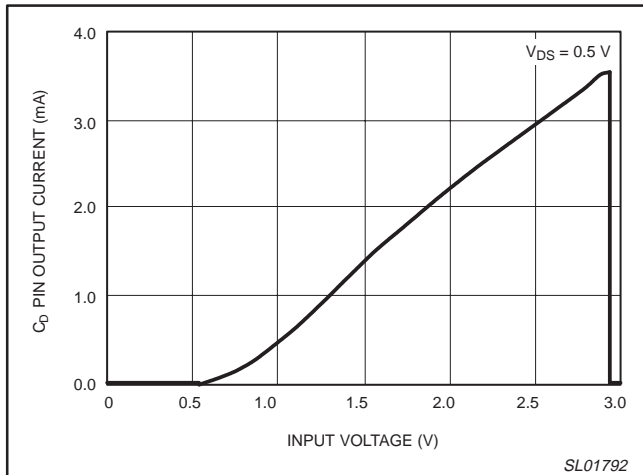
Figure 53. C_D pin output current versus input voltage.
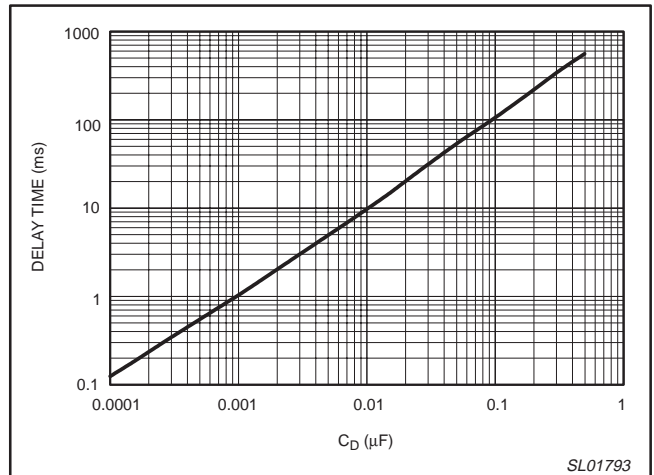
Figure 54. Delay time versus C_D.
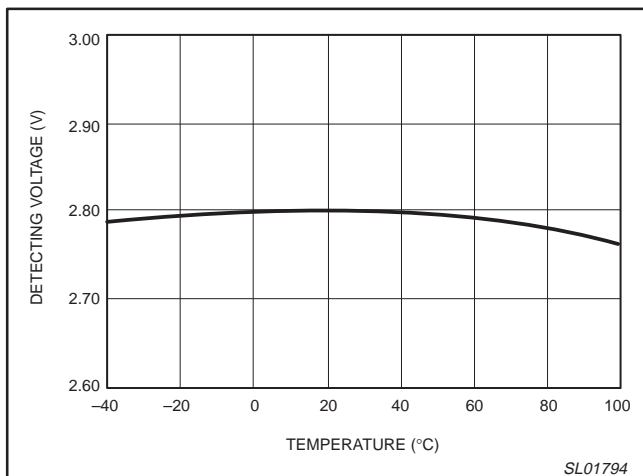
Figure 55. Detection voltage versus temperature.
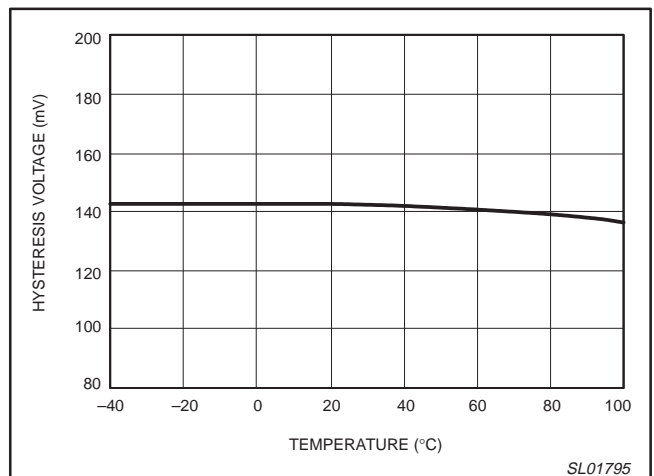
Figure 56. Hysteresis voltage versus temperature.

CMOS system reset with adjustable delay time

TYPICAL PERFORMANCE CURVES *(continued)*
NOTE: Typical characteristics for SA56615-28
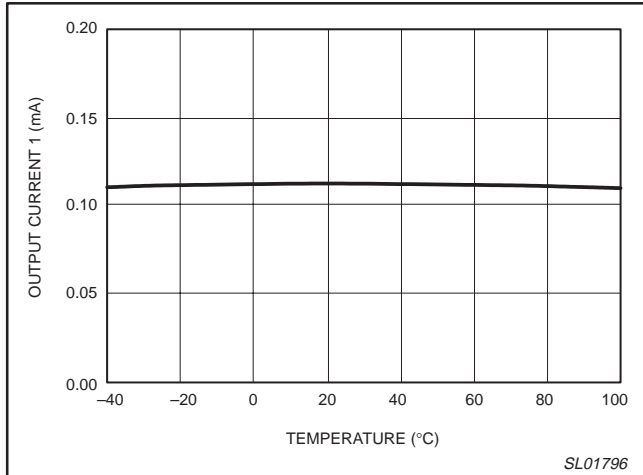
Figure 57. Output current 1 versus temperature.
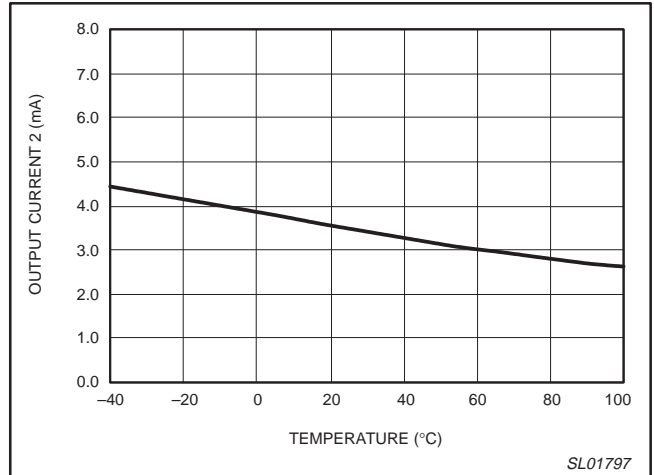
Figure 58. Output current 2 versus temperature.
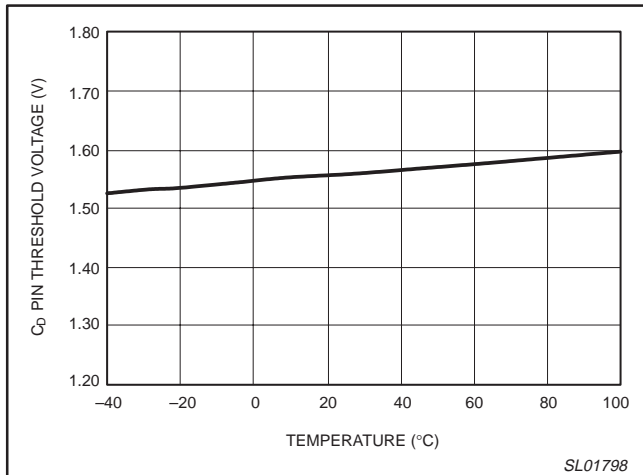
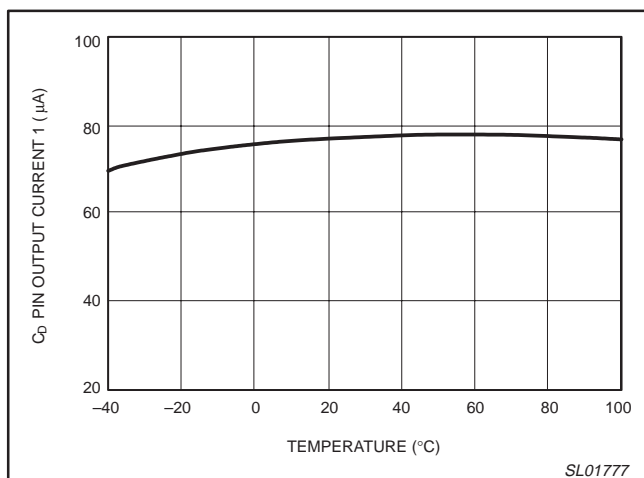**Figure 59. C_D pin threshold voltage versus temperature.**
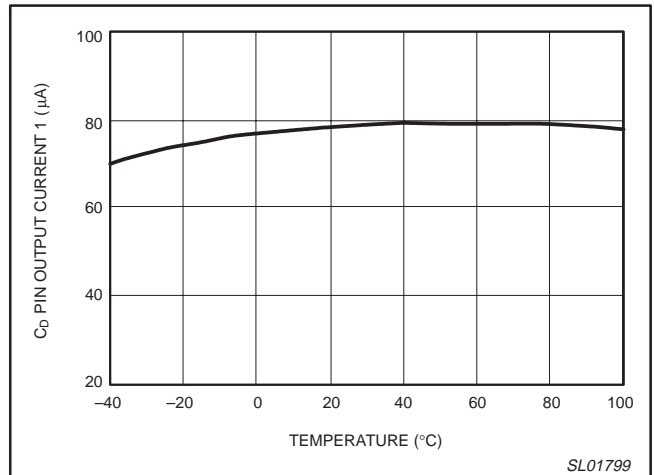
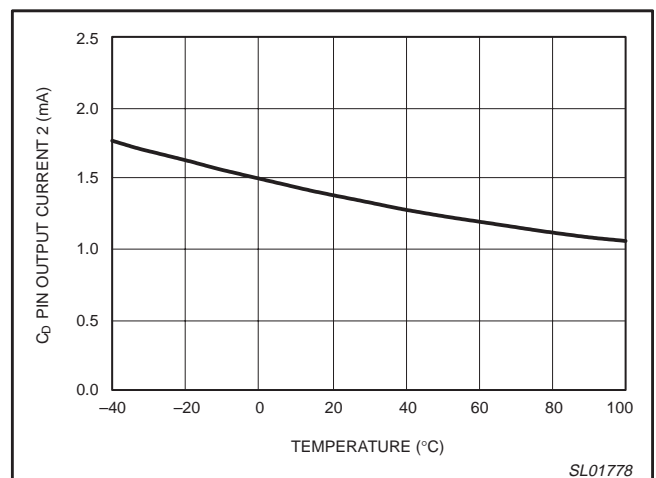**Figure 60. C_D pin output current 1 versus temperature.**
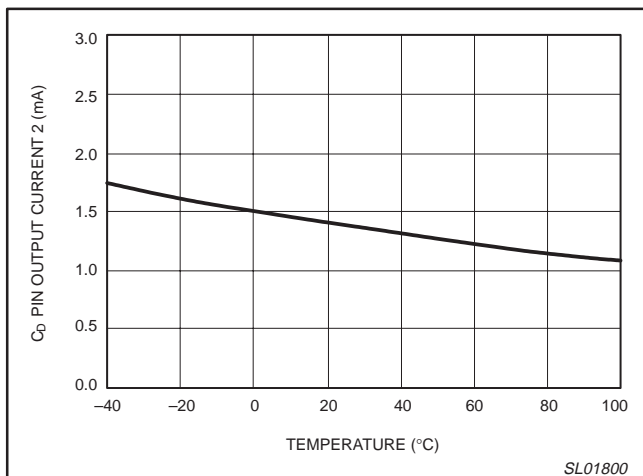
Figure 61. C_D pin output current 2 versus temperature.

TYPICAL PERFORMANCE CURVES (continued)

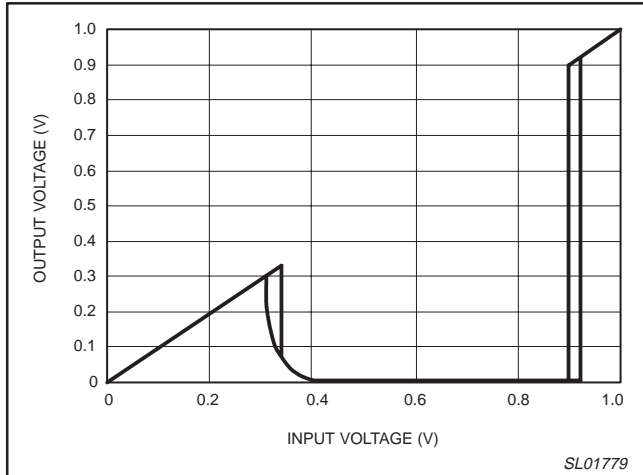**NOTE:** Typical characteristics for SA56615-46
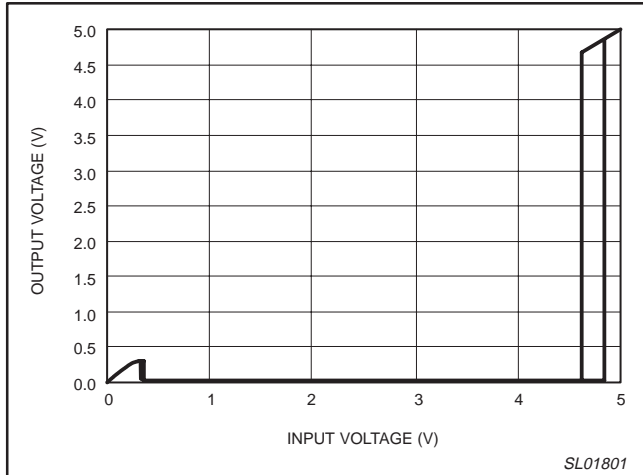
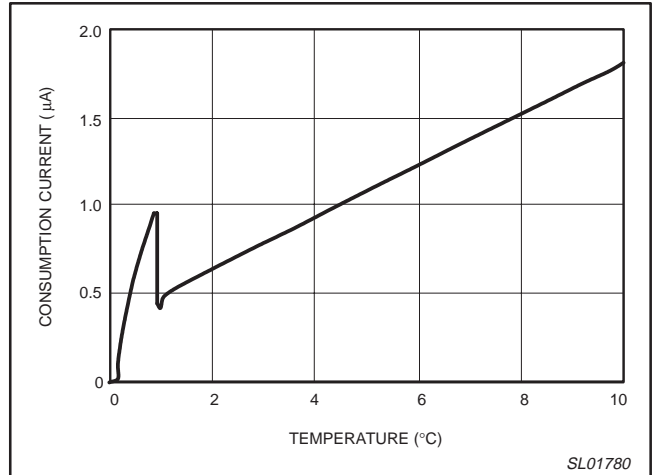**Figure 62. Output voltage versus input voltage.**
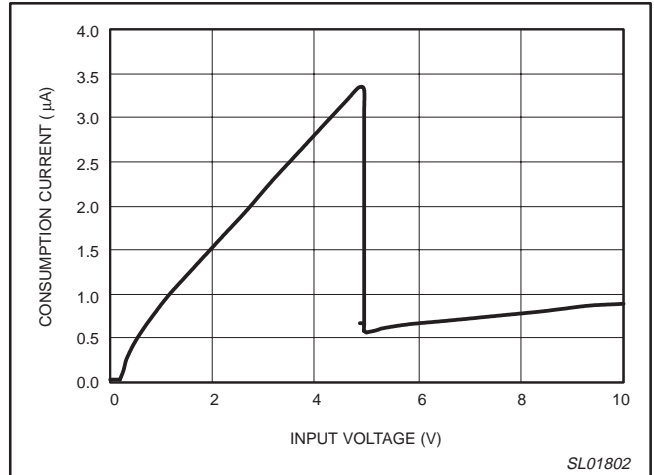
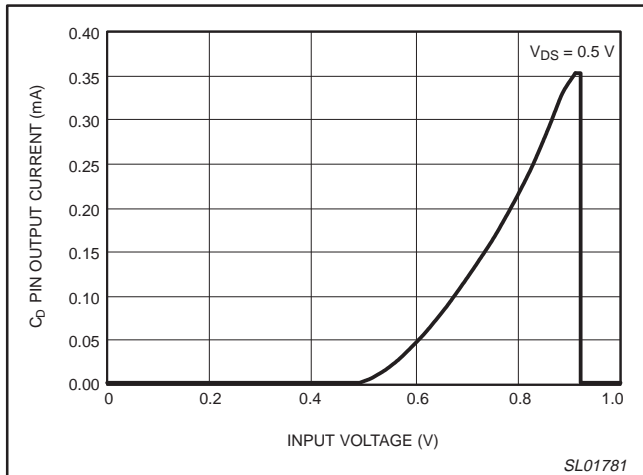**Figure 63. Consumption current versus input voltage.**
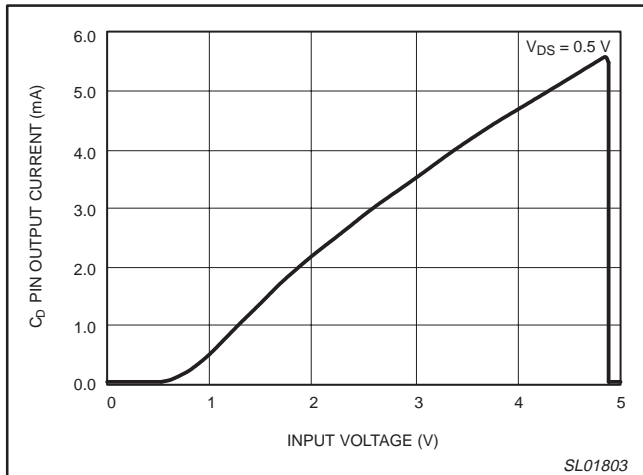
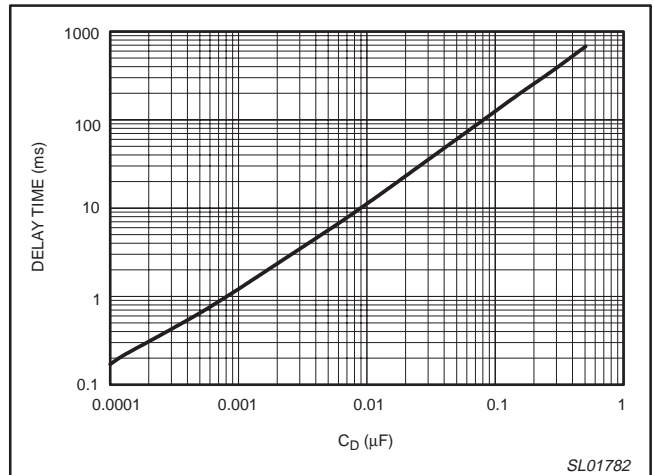**Figure 64. C_D pin output current versus input voltage.**
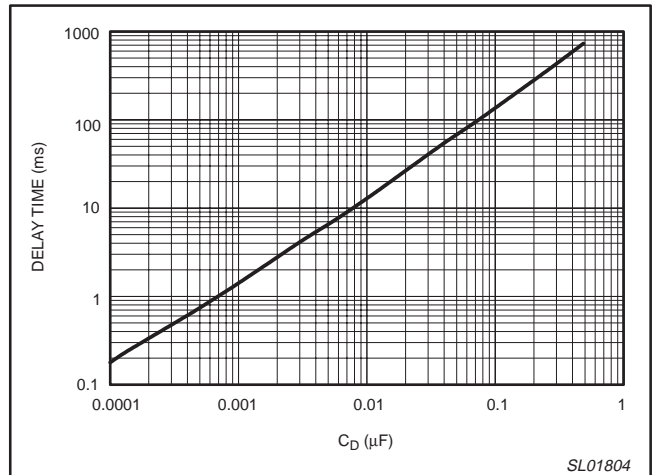
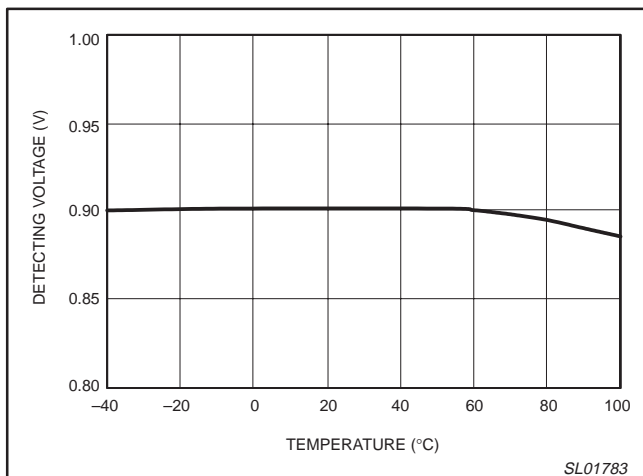**Figure 65. Delay time versus C_D.**
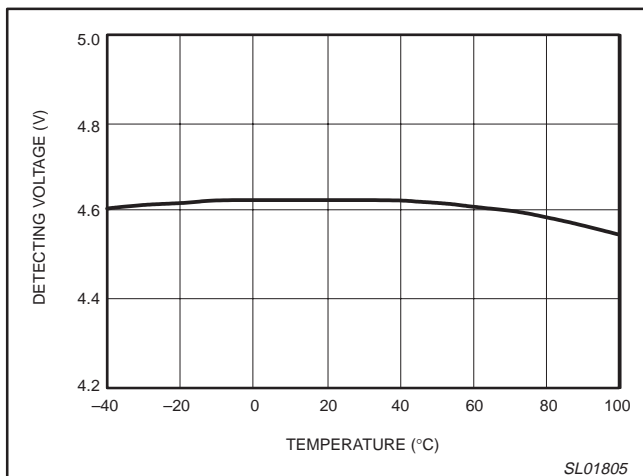
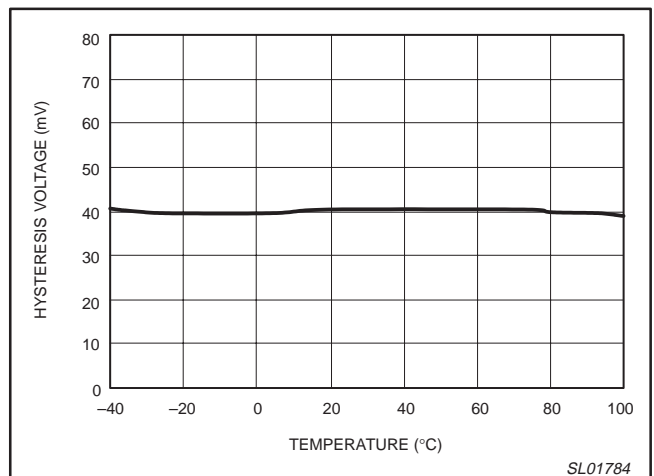
Figure 66. Detection voltage versus temperature.
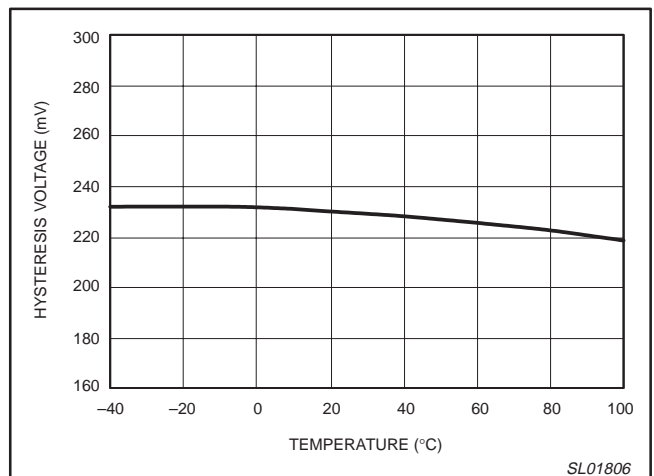
Figure 67. Hysteresis voltage versus temperature.

CMOS system reset with adjustable delay time

TYPICAL PERFORMANCE CURVES (continued)
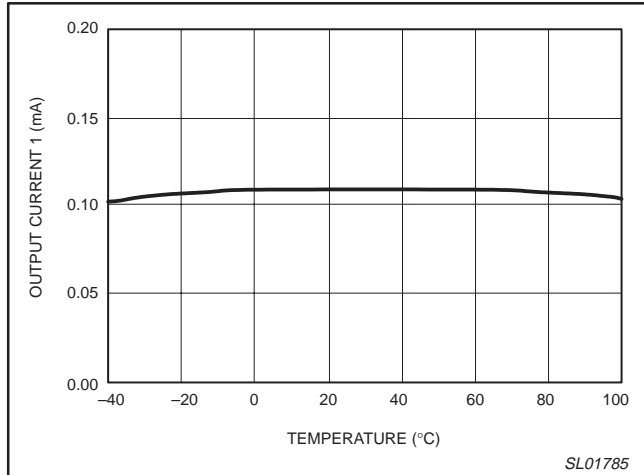**NOTE:** Typical characteristics for SA56615-46
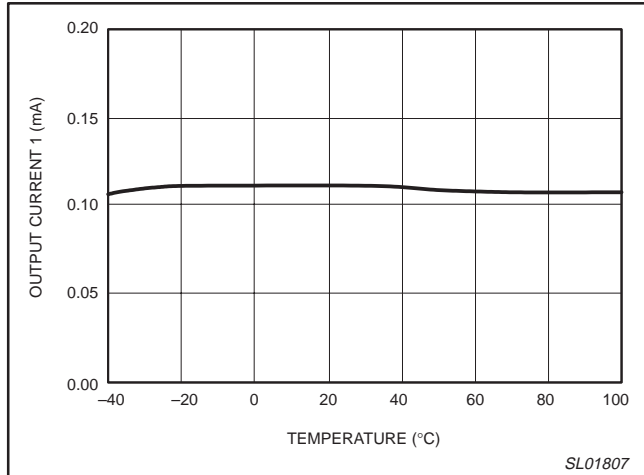
Figure 68. Output current 1 versus temperature.
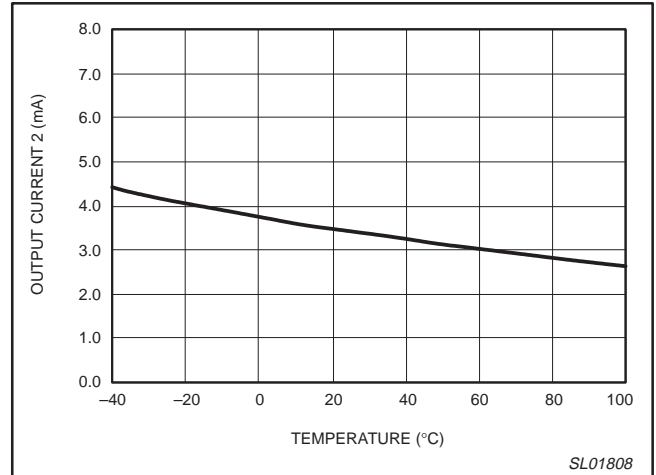
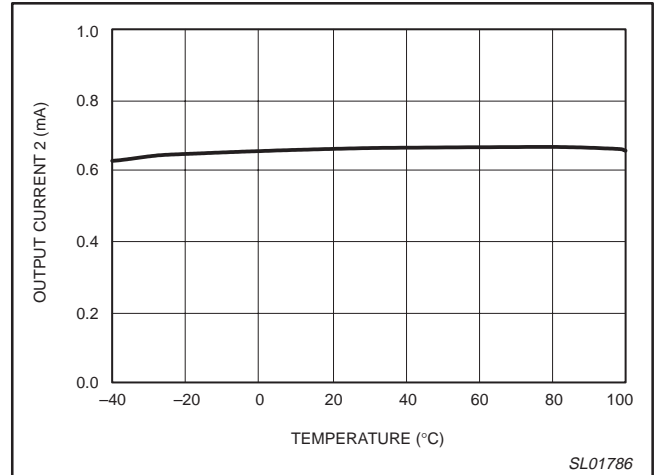
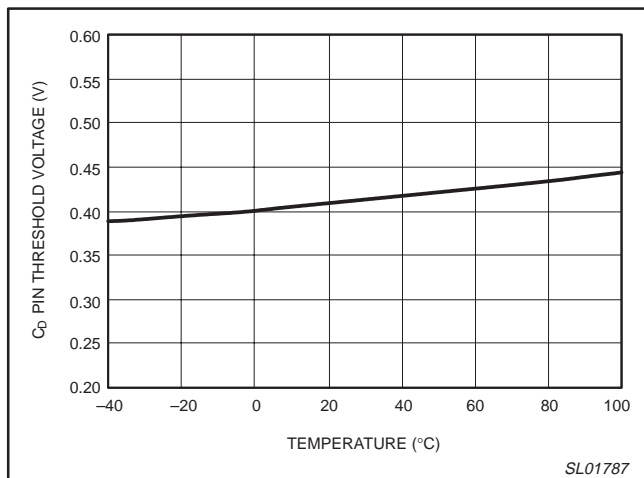**Figure 69. Output current 2 versus temperature.**
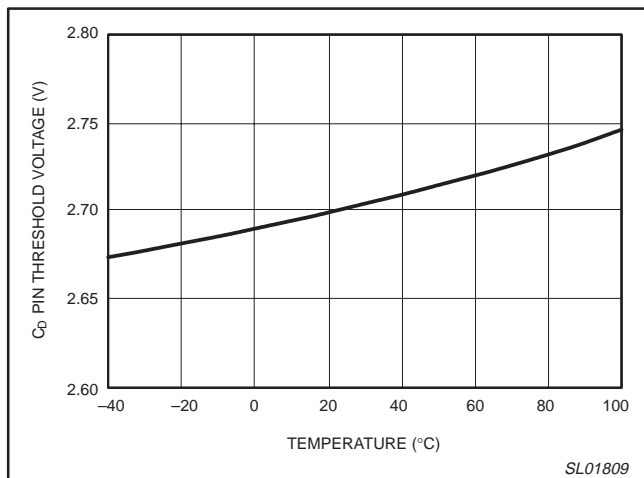
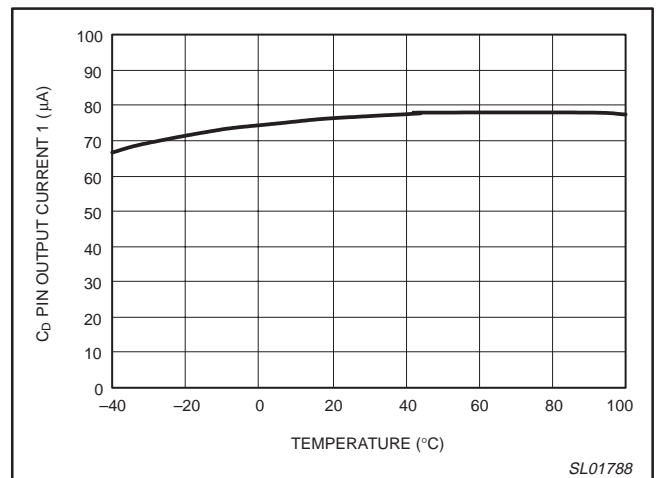**Figure 70. C_D pin threshold voltage versus temperature.**
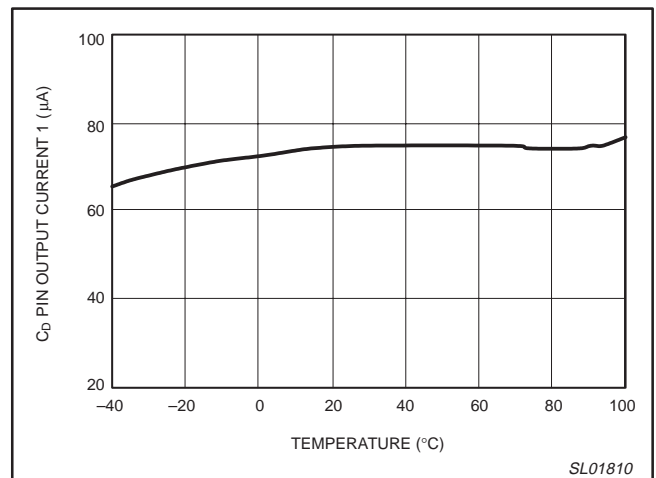
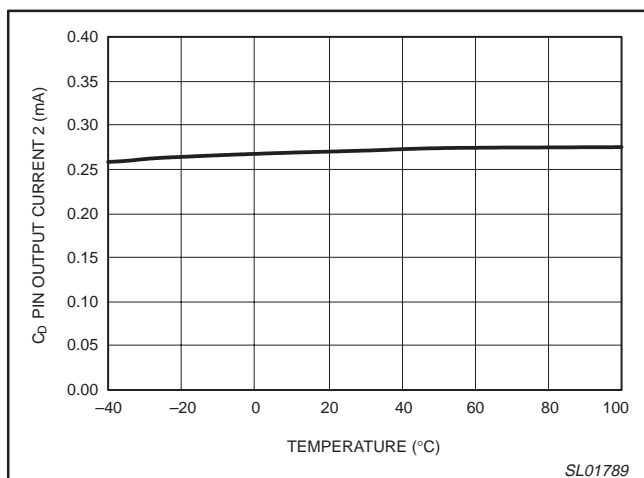
Figure 71. C_D pin output current 1 versus temperature.
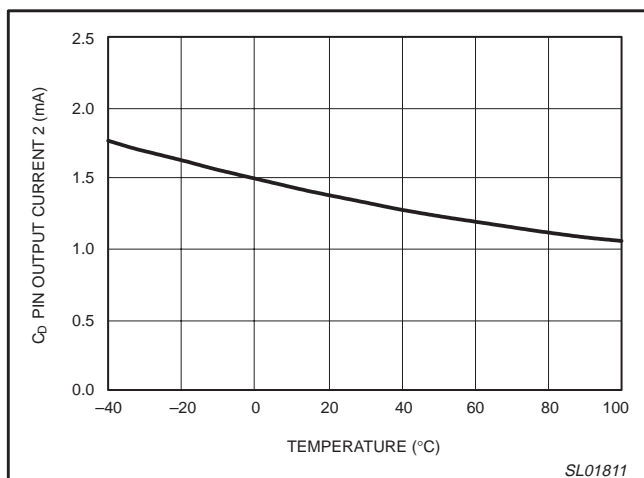
Figure 72. C_D pin output current 2 versus temperature.

CMOS system reset with adjustable delay time

TECHNICAL DISCUSSION

The SA56616-XX and SA56615-XX are CMOS devices designed to monitor the system's power source and provide a system reset function in the event the supply voltage sags below an acceptable level for the system to reliably operate. The SA56616-XX and SA56615-XX generate a compatible reset signal for a wide variety of microprocessors and logic systems. They can operate up to 10 volts. The series includes several versions providing high precision reset threshold levels of 0.9, 1.8, 1.9, 2.0, 2.7, 2.8, 2.9, 3.0, 3.1, 4.2, 4.3, 4.4, 4.5, 4.6, and 4.7 V. The reset threshold incorporates a typical hysteresis of ($V_S \times 0.05$) volts to prevent erratic resets from being generated. The SA56616-XX and SA56615-XX operate at very low supply currents, typically 1.2 μA, while offering high precision of threshold detection, typically $\pm2\%$. They have an on-chip reset time delay which is adjusted by an external capacitor.

The SA56616-XX and SA56615-XX offer different output options; one or the other may be preferred depending on the system criteria. The SA56616-XX (Figure 2) incorporates an active push-pull, Totem-pole output topology comprised of complimentary P-channel and N-channel FETs. A P-channel is on the high supply side and when ON pulls the output to or near the V_{DD} supply voltage from which output source current can be obtained. A complimentary N-channel FET is on the low supply side or ground side, and actively pulls the output LOW or to ground with the capability of sinking current into the output. When connecting the SA56616-XX to a system, the user should be aware of the effect of supplying source current from the output of the SA56616-XX on the system. The SA56615-XX (Figure 1) incorporates a low side N-channel open-drain topology, which requires an external pull-up to V_{DD}. Though this may be regarded as a disadvantage, it is an advantage in many sensitive applications because the open-drain output can not source reset current to a microprocessor when both are operated from a common supply. For this reason, the SA56615-XX offers a safe interconnect to a wide variety of microprocessors.

Figure 73 and Figure 74 are the functional block diagrams of the SA56615-XX and SA56616-XX, respectively. The only difference between them is the output configuration. The internal reference is typically 0.8 V over the operating temperature range. The reference voltage is connected to the non-inverting input of the threshold comparator while the inverting input monitors the supply voltage through a resistor divider network made up of R1, R2, and R3. The output threshold comparator drives the time delay/inverting amplifier network and, in turn, the totem-pole output stage.

When the supply voltage sags to the threshold detection voltage, the resistor divider network supplies a voltage to the inverting input of the threshold comparator which is less than V_{REF}, causing the

output of the comparator to go HIGH. This switches the N-channel FET (M3) to an active ON state, pulling its output (drain) to a low voltage state. The output of M3 is connected to the internal resistor, R_D, the time delay pin C_D, and the input of the inverting amplifier. The output level of the C_D pin will rise to the level of V_{TCD} by the time constant formed by internal R_D to V_{DD} and external C_D to ground. The output of the inverting amplifier will then be pulled to a LOW state. This causes the high side FET M1 of the totem-pole output stage to turn off while simultaneously turning the low side N-channel FET M2 to an active ON state, pulling the output to a low voltage state.

The device adheres to true input/output logic protocol. The output goes to a low voltage state when the input is LOW (below V_{SL}) and the output goes HIGH when the input is HIGH (above V_{SH}).

The low side N-channel FET (M4) establishes threshold hysteresis by turning ON whenever the threshold comparator output goes to a HIGH state (when V_{DD} sags to or below the V_{SL} level). With M4 in the ON state, additional current flows through resistors R1 and R2 which causes the inverting input of the threshold comparator to be pulled even lower. For the comparator to reverse its output polarity and turn OFF M4, the V_{DD} source voltage must overcome this additional pull-down voltage on the comparator's inverting input. The differential voltage required to do this establishes the hysteresis voltage of the sensed threshold voltage. Typically, this is ($V_S \times 0.5$) volts.

When the V_{DD} voltage sags and is at or below the Detection Threshold (V_{SL}), the device will assert a Reset Low output at or very near ground potential. As the V_{DD} voltage rises from ($V_{DD} < V_{SL}$) to V_{SH} or higher, the reset is released and the output follows V_{DD}. Conversely, decreases in V_{DD} from ($V_{DD} > V_{SL}$) to V_{SL} or lower cause the output to be pulled to ground.

Hysteresis Voltage = Release Voltage – Detection Threshold Voltage

$$V_{hys} = V_{SH} - V_{SL}$$

where:

$$V_{SH} = V_{SL} + V_{hys} = V_{REF}(R1 + R2)/R2$$

$$V_{SL} = V_{REF}(R1 + R2 + R3)/(R2 + R3)$$

When V_{DD} drops below the minimum operating voltage, typically less than 0.95 volts, the output is undefined and output reset low assertion is not guaranteed. At this level of V_{DD} the output will try to rise to V_{DD}.

The V_{REF} voltage is typically 0.8 V. The devices are fabricated using a high resistance CMOS process and utilize high resistance R1, R2, and R3 values requiring very small amounts of current. This combination achieves very efficient low power performance over the full temperature.
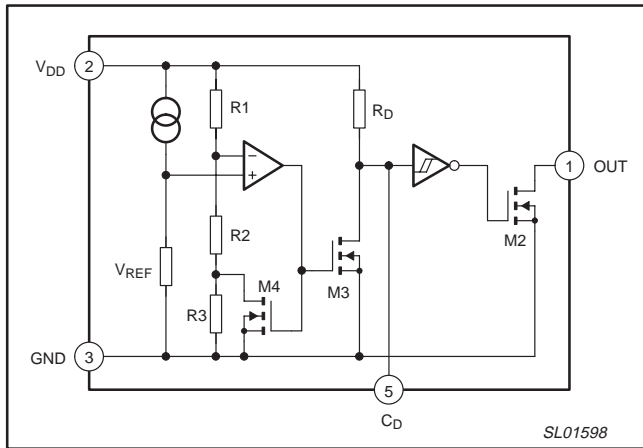
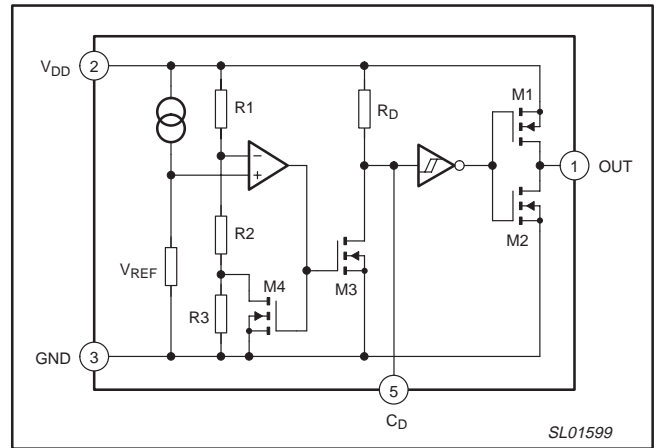## Equivalent circuit diagrams

Figure 73. SA56615-XX equivalent circuit.

Figure 74. SA56616-XX equivalent circuit.

CMOS system reset with adjustable delay time

TIMING DIAGRAM

The Timing Diagram shown in Figure 75 depicts the operation of the device. Letters A – K on the TIME axis indicate specific events.

A: At "A", V_{DD} begins to increase. Initially, the V_{OUT} voltage increases but abruptly decreases when V_{DD} reaches the level (approximately 0.8 V) that activates the internal bias circuitry and $\overline{RESET}$ is asserted.

B: At "B", V_{DD} reaches the high side threshold level, V_{SH}. At this point the reset delay timer is initiated and V_{TCD}, delay pin threshold voltage begins to rise. V_{DD} increases to its nominal operating level without releasing the reset.

C: At "C", the delay pin threshold voltage is reached, and the IC releases the hold on the V_{OUT} reset. The reset output voltage goes to V_{DD}.

D–E: At "D", V_{DD} begins to fall, causing the reset output to follow. V_{DD} continues to fall until the V_{SL}, low side detection threshold level is reached at "E". This causes the a reset signal to be generated (V_{OUT} reset goes LOW).

E–F: Between "E" and "F", V_{DD} starts rising.

F–G: At "F", V_{DD} rises to V_{SH}. Once again, the IC initiates the reset delay timer and V_{TCD} starts to rise until the delay pin threshold level is reached and the IC releases the hold on the V_{OUT} reset. At "G", the reset output V_{OUT} goes to V_{DD}.

G–H: Between "G" and "H", V_{OUT} follow V_{DD}. As long V_{DD} remains above V_{SH}, no reset signal will be triggered. Before V_{DD} falls to the V_{SH} threshold, it begins to rise, causing V_{OUT} to follow it. At "H" V_{DD} returns to its nominal operating level.

J: At "J" V_{DD} falls until the V_{SL} threshold point is reached. At this level, a $\overline{RESET}$ signal is generated and V_{OUT} goes LOW.

K: At "K", the V_{DD} voltage has decreased until normal internal circuit bias is unable to maintain a V_{OUT} reset. As a result, V_{OUT} may rise to less than 0.8 V. As V_{DD} decreases further, V_{OUT} reset also decreases to zero.
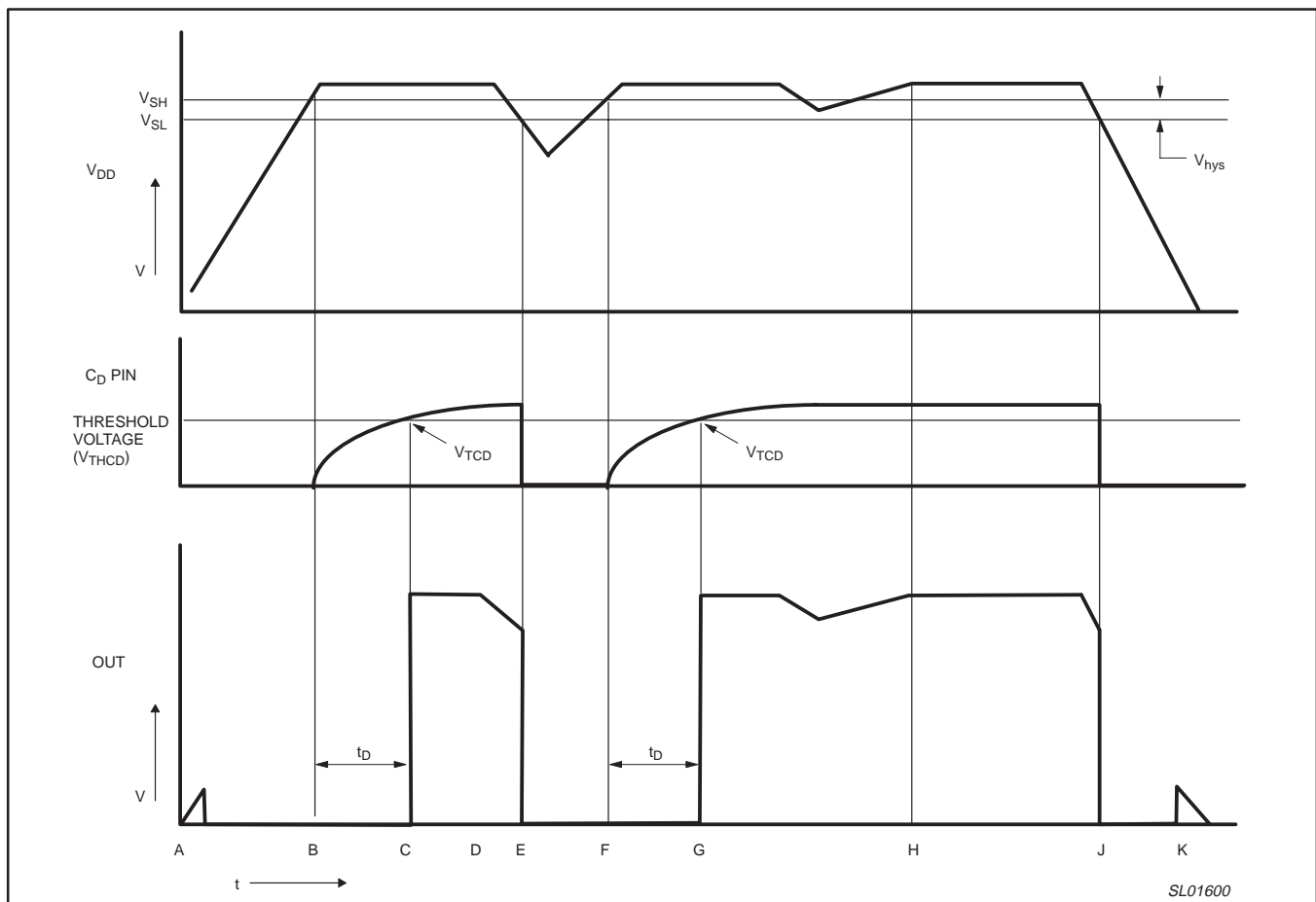

Figure 75. Timing diagram.

APPLICATION INFORMATION

The SA56615-XX differs from the SA56616-XX in that it requires a V_{OUT} ($\overline{RESET}$) pull-up resistor from pin 1 to V_{DD}. Typical value for R_{PU}, the pull-up resistor, is 470 kΩ.

The reset delay time is the duration measured from the time V_{DD} exceeds the upper detection threshold (V_{SH}) and when reset release occurs (V_{OUT} or $\overline{RESET}$ goes HIGH).

Figures 76 and 77 show typical application circuits for the SA56615-XX and SA56616-XX in which the delay time is externally adjusted by a capacitor connected from C_D (pin 5) to ground. The delay time may be varied from 150 ns to 1 second with the appropriate external capacitor. Typical capacitor value is from 100 pF to 1 μF. Refer to "Delay time versus C_D" in Typical Performance Curves for the various detection threshold voltages.

The delay time is approximated by

$$t_D \sim 1.2 \times R_D \times C_D$$

where:
    R_D is C_D pin resistance (typically 1 MΩ)
    C_D is the external delay time capacitor

The C_D (delay pin) threshold voltage, V_{TCD} is typically $0.5 \times V_{DD}$. Figures 78 and 79 show the test circuits that are used to measure the reset delay time of the SA56615-XX and SA56616-XX respectively. The delay diagrams indicate how the measurement is to be made. The input voltage, V_{IN} is switched from V_{SH} + 2.0 V to 0.7 V. The delay time is measured from the falling edge of V_{IN} to where the C_D (delay pin) threshold voltage is $0.5 \times V_{DD}$.
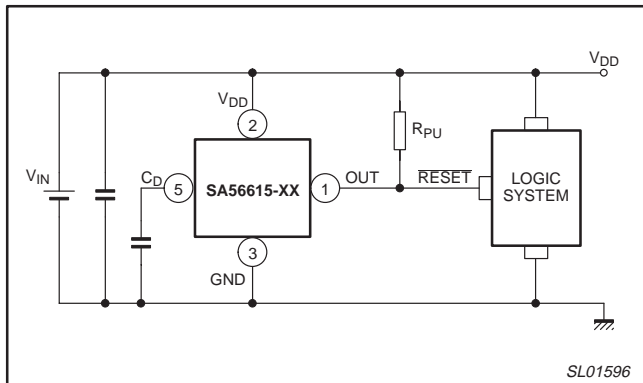

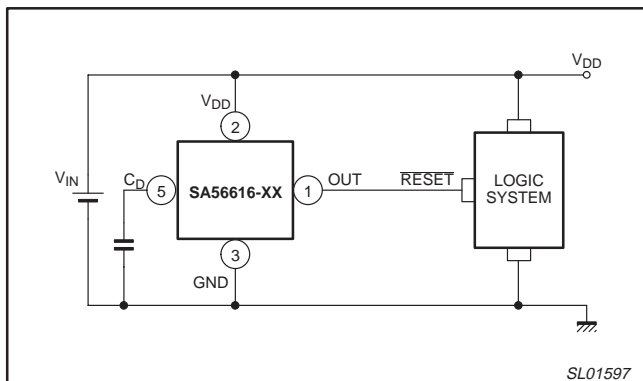**Figure 76. SA56615-XX application circuit.**

Figure 77. SA56616-XX application circuit.

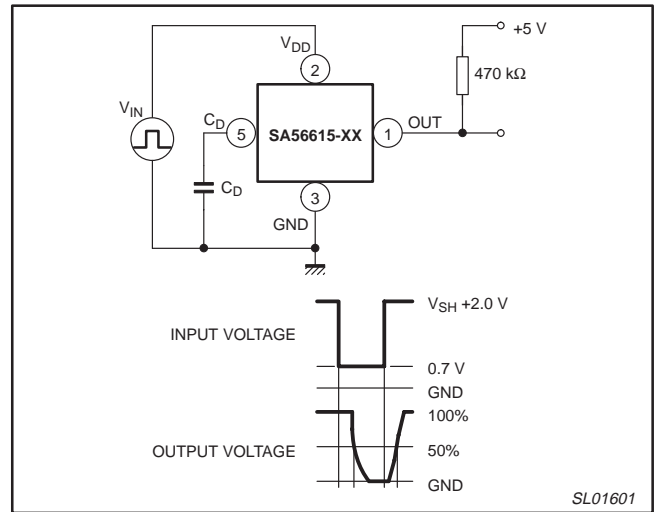**Figure 78. SA56615-XX delay time, t_D test circuit and diagram.**
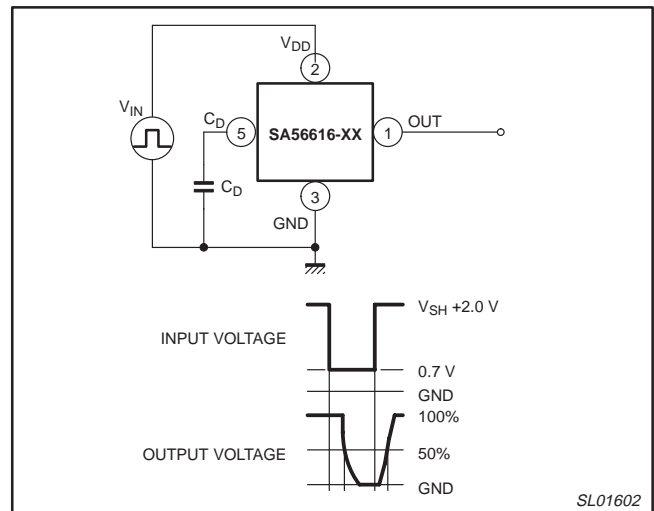
Figure 79. SA56616-XX delay time, t_D test circuit and diagram.

PACKING METHOD

The SA56615-XX and SA56616-XX are packed in reels, as shown in Figure 80.
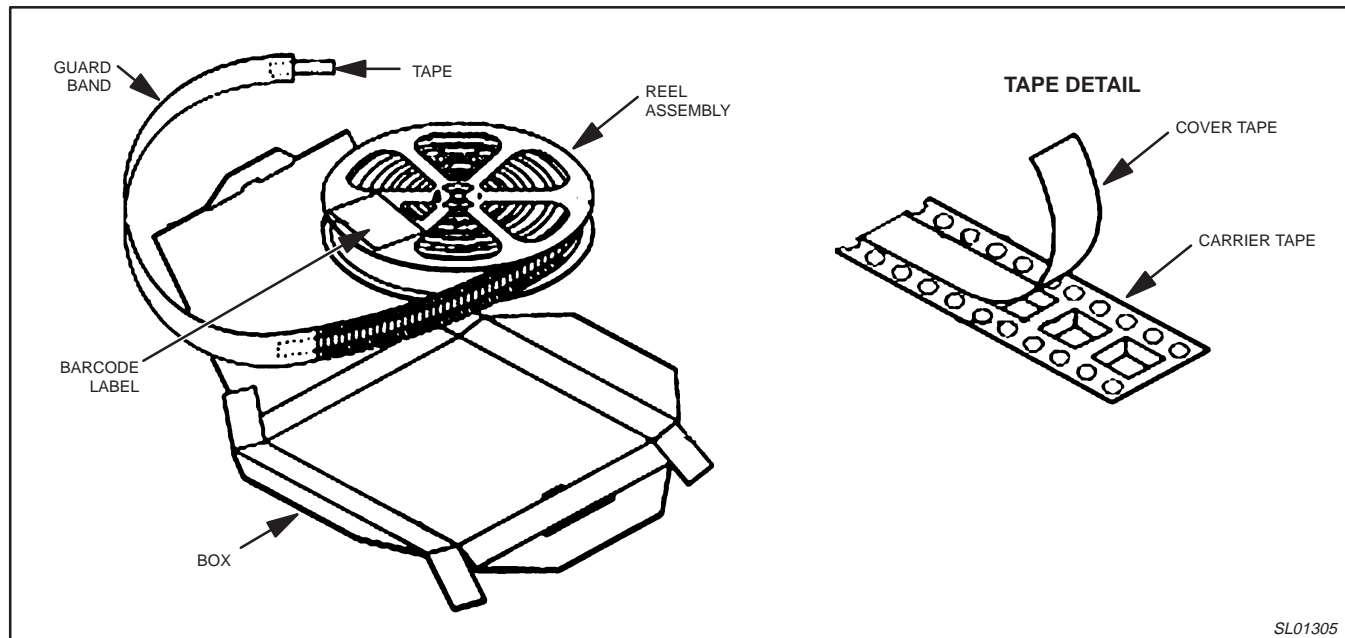
Figure 80. Tape and reel packing method.

SOT23-5: plastic small outline package; 5 leads; body width 1.5 mm

detail X

0   1   2 mm
scale
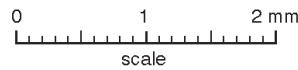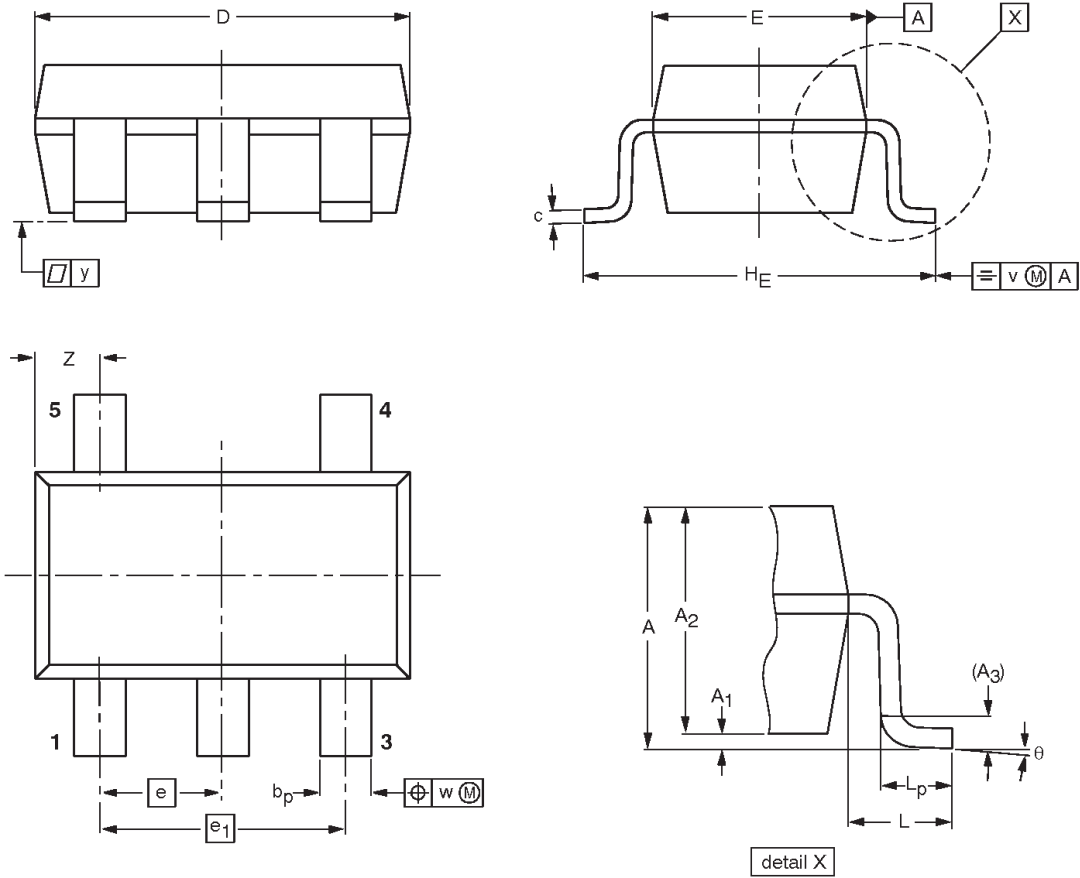
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A1	A2	A3	bp	c	D(1)	E(1)	e	e1	HE	L	Lp			y		θ
mm	1.35	0.05 0.15	1.2 1.0	0.025	0.55 0.41	0.22 0.08	3.00 2.70	1.70 1.50	0.95	1.90	3.00 2.60	0.60	0.55 0.35			0.1		8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			
	IEC	JEDEC	EIAJ	
		MO-178		

NOTES

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Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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